

Amendments to the Drawings:

Formal replacement drawings are submitted herewith to replace the drawings currently on file. Changes to the figures have been made to correct clerical errors and all changes are noted in the attached annotated sheet. Approval by the Examiner is respectfully requested.

Attachment: Replacement Figures 1-5

Annotated Figures 1-5

REMARKS

The Office Action dated September 29, 2004 has been received and reviewed by the applicant. Claims 1-40 are in the application. Claims 1-9, 11-13, 16-19, 21-25, 27 and 30-34 stand rejected and claims 10, 14, 15, 20, 26, 28 and 29 stand objected to. Claims 35-40 have been cancelled in response to a restriction requirement.

Claims 1, 5-9, 12, 13, 16-19, 21-25, 27 and 30-34 stand rejected under 35 USC 102(a) as anticipated by Dan (JP 10186072, dated July 1, 1998).

Claims 2-4, 11 and 34 stand rejected under 35 USC 103(a) as unpatentable over Dan (JP 10186072).


Independent claims 1, 19 and 27 were rejected as being anticipated by Dan. Claim 1 has been amended herein to require that the first interface and the second interface are independent of each other. Claim 19 has been amended herein to recite that the processor bus interface is independent of the image bus interface, the processor bus interface and the image bus interface operating in parallel. Similarly, claim 27 has been amended herein to require the processor bus interface to be independent of the image bus interface, the processor bus interface and the image bus interface connected in parallel to the host processing system. Figure 1 of the present application shows the configuration used in prior art, in which a single bus interface (12) and a single local communications bus (13) are used to carry both image data and processing instructions sent from bus (14) of the host computer. Looking at Figure 2 of the present application, it can be seen that the present invention includes a first interface (122) and a second interface (142) coupled to the host processing system (90). From page 7, lines 21-27 it can be seen that the first interface (122) is adapted for receiving raw image data and the second interface (142) is adapted for communicating processing instructions between a processor and the host processing system (90).

The cited figure in the Dan reference clearly shows only a single communication cable between the host machine (3) and the controller (2). In this way, it is similar to figure 1 of the present application, which is designated as prior art. Therefore, the Examiner's position stated at the top of page 5 with regard to the Dan reference is incorrect. Dan teaches that the second interface (8) is coupled to the host through the same bus as the first interface (5), not separately, as required by

claims 1, 19 and 27 of the present application. Dan neither teaches nor suggests a first bus for the transmission of image data signals from the host processing system and a second bus for transmission of processor instruction signals from the host processing system wherein the first bus is independent from the second bus. Therefore, claims 1, 19 and 27 as amended are clearly allowable over Dan.

For the reasons set forth above, it is believed that the application is in condition for allowance. Accordingly, reconsideration and favorable action are respectfully requested.

Respectfully submitted,


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If the Examiner is unable to reach the Applicant(s) Attorney at the telephone number provided, the Examiner is requested to communicate with Eastman Kodak Company Patent Operations at (585) 477-4656.

Enclosures: Replacement Figure 2
Annotated Sheet Showing Changes



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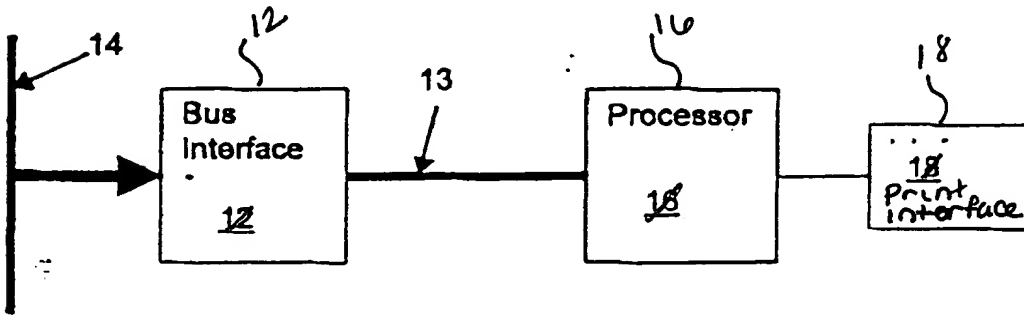


Figure 1
(Prior Art)



Appl. No. 09/745,027
Amdt. Dated December 10, 2004
Reply to Office Action of September 29, 2004
Annotated Sheet

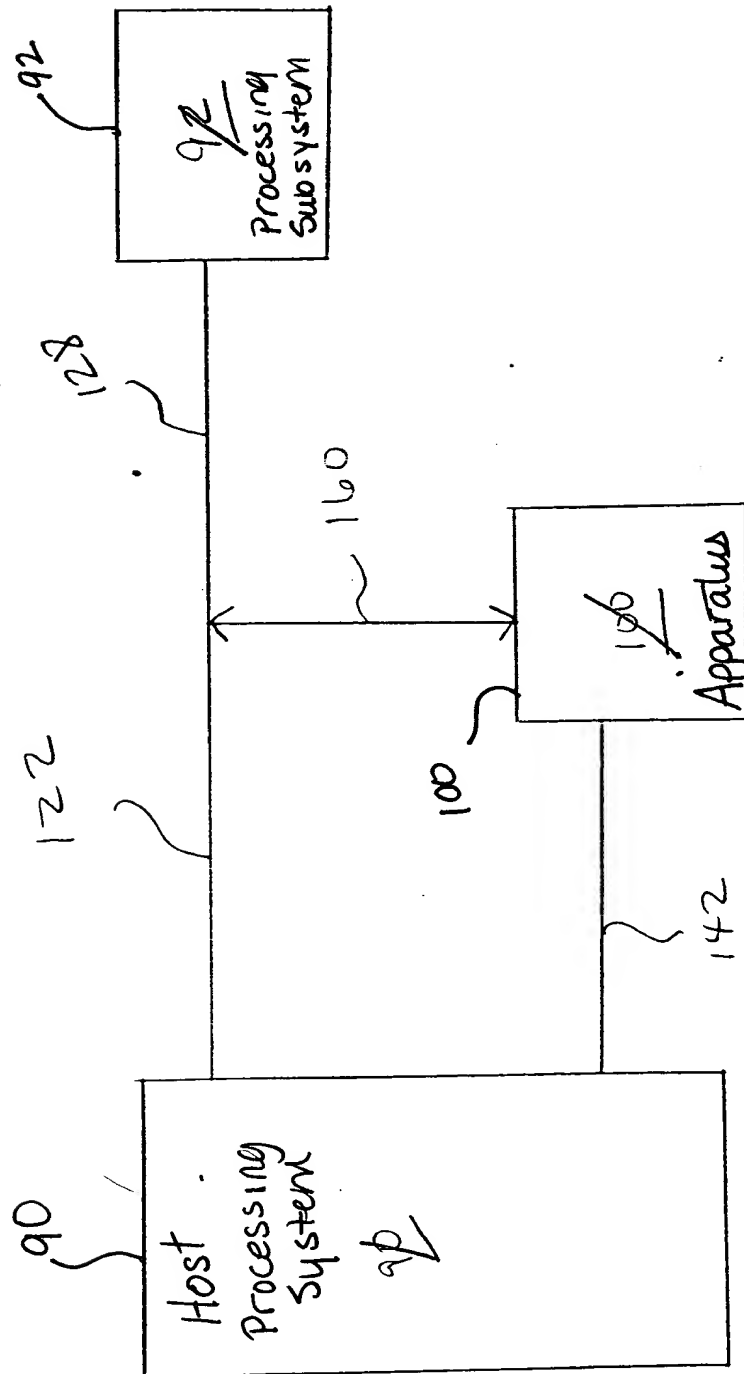


Figure 2

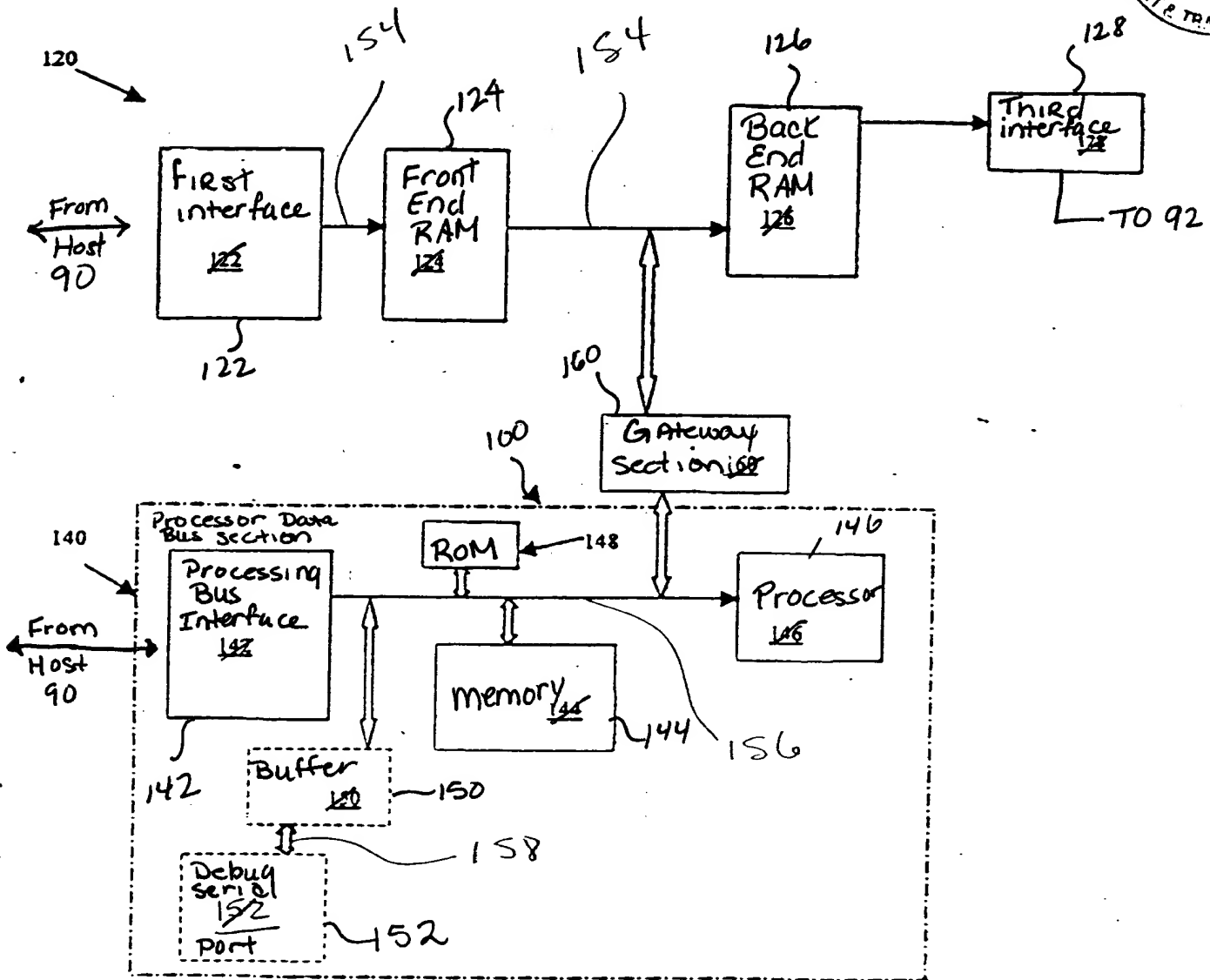
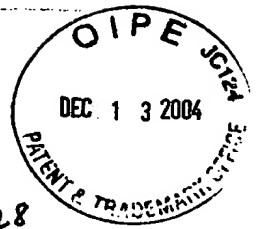
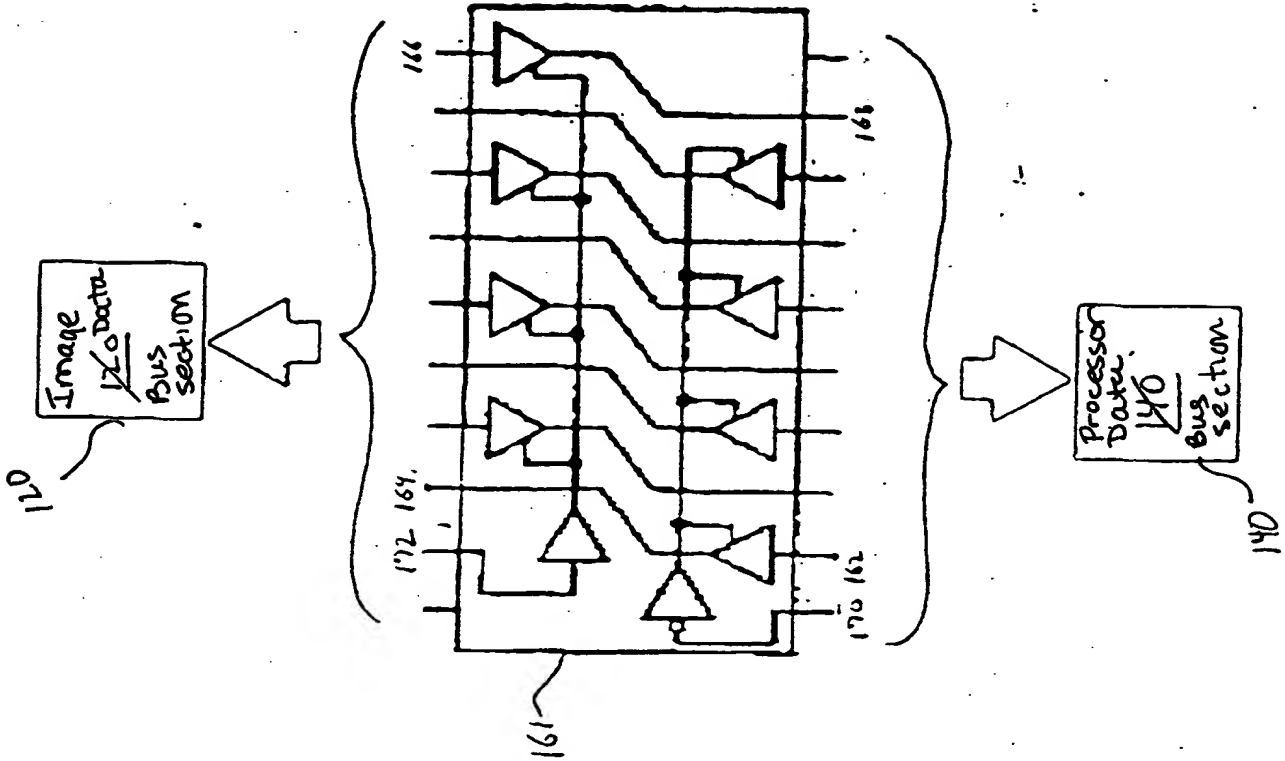


Figure 3



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Figure 4

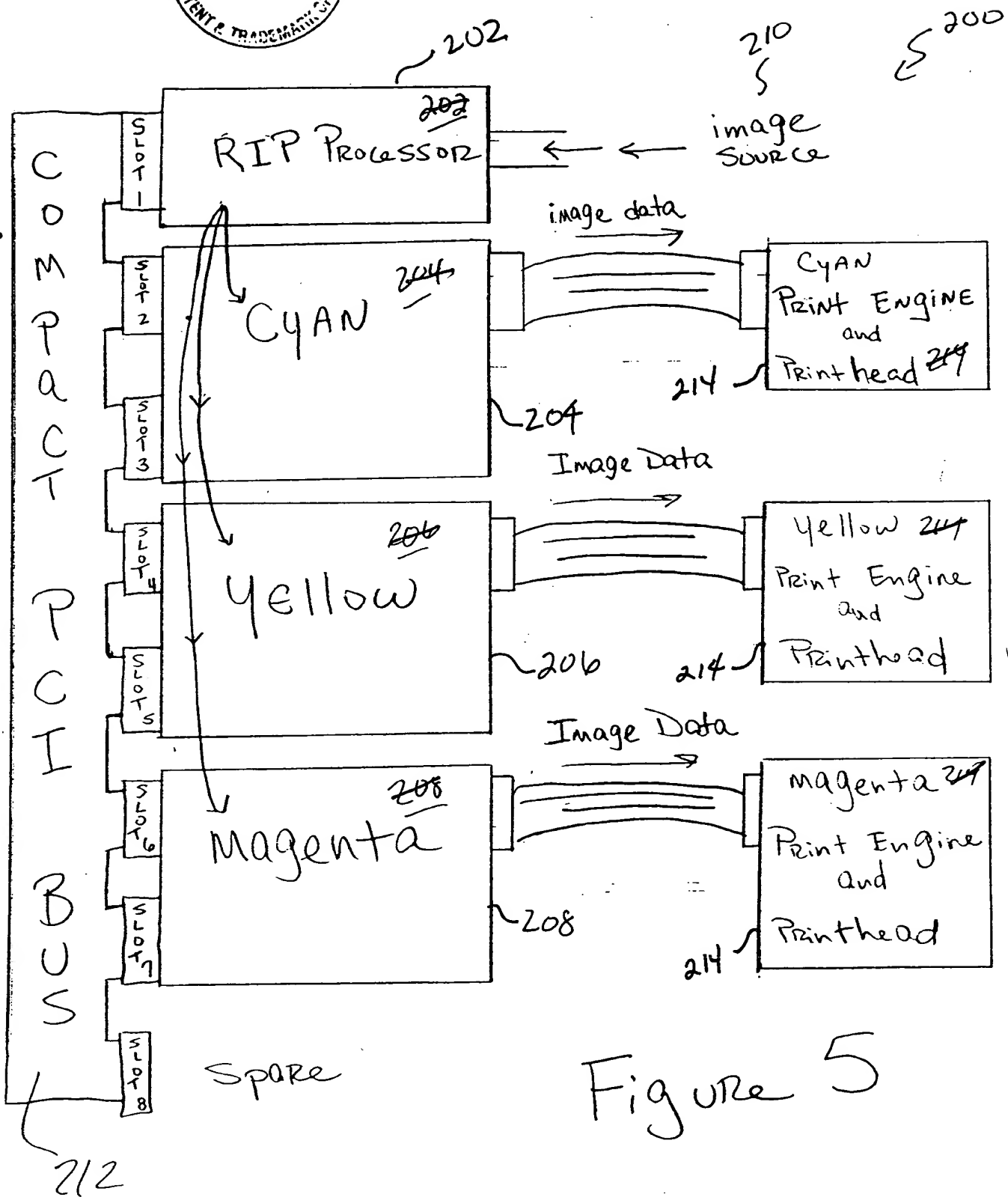


Figure 5